

RECEIVED  
CENTRAL FAX CENTER  
AUG 29 2003

IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

Applicant: Avery, et al. Case: SAR 14179  
Serial No.: 10/077,833 Filed: November 5, 2001  
Examiner: Tran, Tan N. Group Art Unit: 2826  
Title: **SILICON CONTROLLED RECTIFIER ELECTROSTATIC  
DISCHARGE PROTECTION DEVICE WITH EXTERNAL ON-CHIP  
TRIGGERING AND COMPACT INTERNAL DIMENSIONS FOR  
FAST TRIGGERING**

COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

SIR:

DECLARATION UNDER 37 C.F.R. § 1.131

We, Leslie R. Avery, John Armer, and Koen G. M. Verhaeghe, hereby declare as follows:

1. That we are the inventors of the above-captioned patent application who are presently available to execute this declaration; and that inventors Christian C. Russ and Markus P. J. Mergens have moved to Germany and are not available to execute this declaration;
2. That we are inventors of the subject matter described and claimed in the present application and are familiar with the disclosure and pending claims, and that the disclosure of the present application describes an invention that was conceived prior to October 10, 2001;
3. That rejected claims 1-23 define embodiments that were conceived prior to October 10, 2001, and constructively reduced to practice by describing the embodiments in the present patent application filed November 5, 2001, as evidenced by Exhibits A-E;
4. That the subject matter of claims 1-23 was diligently pursued by Applicants from a time beginning before October 10, 2001, until filing of the present patent application on November 5, 2001, or any earlier actual reduction to practice;
5. Exhibits A through E are enclosed herewith in support of declaration that we conceived of and reduced to practice the present invention in this country on

37 C.F.R §1.131 Declaration  
Serial Number: 10/077,833

or before the publication date of the U.S. patent publication U.S. 2002/0041007 A1 by "Russ", filed October 10, 2001 and published April 11, 2002;

6. Exhibit A is a copy of a test data sheet including test structure analysis data for a grounded-gate silicon controlled rectifier (GGSCR) of the present invention;

7. Exhibit B is a copy of page 11 from a document entitled "TBS CMSO2 RF ESD test chip" describing various GGSCR structures of the present invention on a test chip;

8. Exhibit C is a copy of page 13 from the document entitled "TBS CMSO2 RF ESD test chip" depicting a layout example of the GGSCR of the present invention, where the GGSCR includes an external trigger GGNMOS device coupled to an SCR of the present invention.

9. Exhibit D is a copy of page 24 from a document entitled "C10N 2kV ESD design Guidelines, Bus Concepts, and Circuits" depicting various schematics of the GGSCR structures of the present invention for different supply voltage environments;

10. Exhibit E is a copy of page 25 from the document entitled "C10N 2kV ESD design Guidelines, Bus Concepts, and Circuits" depicting a cross-sectional view and layout details of the GGSCR having an external, on-chip, trigger GGNMOS coupled to the SCR of the present invention; and

11. That the disclosures of Exhibits A-E are dated prior to October 10, 2001.

The undersigned, Leslie R. Avery, John Armer, and Koen G. M. Verhaege, hereby declare that all statements made herein of our own knowledge are true and that these statements made on information and belief are believed to be true and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent resulting therefrom.

July 29, 2003  
Date

Leslie Ronald Avery  
Leslie R. Avery

7-28-2003  
Date

John Armer  
John Armer

8-20-2003  
Date

Koen G. M. Verhaege  
Koen G. M. Verhaege

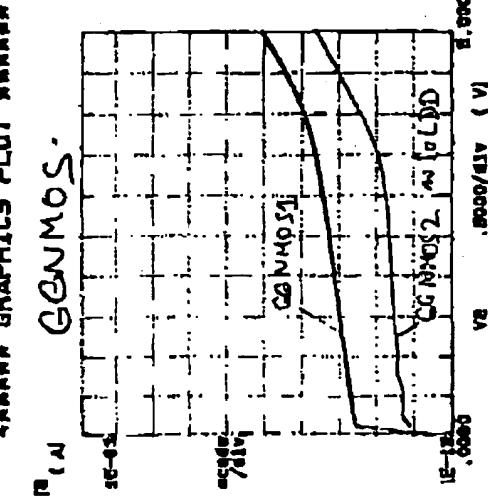
EXHIBIT A

H7L7 Houseshot

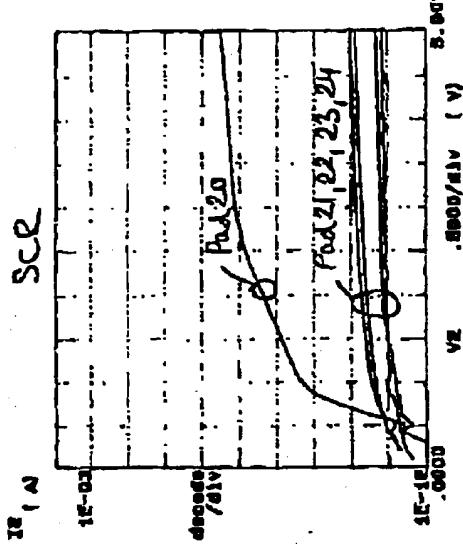
all vs GND (p.20)

T1 (=NOSE)

GEMOS



GRAPHICS PLOT



T1

GEMOS

SCR

T2

GEMOS

SCR

T3

GEMOS

SCR

T4

GEMOS

SCR

T5

GEMOS

SCR

T6

GEMOS

SCR

T7

GEMOS

SCR

T8

GEMOS

SCR

T9

GEMOS

SCR

T10

GEMOS

SCR

T11

GEMOS

SCR

T12

GEMOS

SCR

T13

GEMOS

SCR

T14

GEMOS

SCR

T15

GEMOS

SCR

T16

GEMOS

SCR

T17

GEMOS

SCR

T18

GEMOS

SCR

T19

GEMOS

SCR

T20

GEMOS

SCR

T21

GEMOS

SCR

T22

GEMOS

SCR

T23

GEMOS

SCR

T24

GEMOS

SCR

T25

GEMOS

SCR

T26

GEMOS

SCR

T27

GEMOS

SCR

T28

GEMOS

SCR

T29

GEMOS

SCR

T30

GEMOS

SCR

T31

GEMOS

SCR

T32

GEMOS

SCR

T33

GEMOS

SCR

T34

GEMOS

SCR

T35

GEMOS

SCR

T36

GEMOS

SCR

T37

GEMOS

SCR

T38

GEMOS

SCR

T39

GEMOS

SCR

T40

GEMOS

SCR

T41

GEMOS

SCR

T42

GEMOS

SCR

T43

GEMOS

SCR

T44

GEMOS

SCR

T45

GEMOS

SCR

T46

GEMOS

SCR

T47

GEMOS

SCR

T48

GEMOS

SCR

T49

GEMOS

SCR

T50

GEMOS

SCR

T51

GEMOS

SCR

T52

GEMOS

SCR

T53

GEMOS

SCR

T54

GEMOS

SCR

T55

GEMOS

SCR

T56

GEMOS

SCR

T57

GEMOS

SCR

T58

GEMOS

SCR

T59

GEMOS

SCR

T60

GEMOS

SCR

T61

GEMOS

SCR

T62

GEMOS

SCR

T63

GEMOS

SCR

T64

GEMOS

SCR

T65

GEMOS

SCR

T66

GEMOS

SCR

T67

GEMOS

SCR

T68

GEMOS

SCR

T69

GEMOS

SCR

T70

GEMOS

SCR

T71

GEMOS

SCR

T72

GEMOS

SCR

T73

GEMOS

SCR

T74

GEMOS

SCR

T75

GEMOS

SCR

T76

GEMOS

SCR

T77

GEMOS

SCR

T78

GEMOS

SCR

T79

GEMOS

SCR

T80

GEMOS

SCR

T81

GEMOS

SCR

T82

GEMOS

SCR

T83

GEMOS

SCR

T84

GEMOS

SCR

T85

GEMOS

SCR

T86

GEMOS

SCR

T87

GEMOS

SCR

T88

GEMOS

SCR

T89

GEMOS

SCR

T90

GEMOS

SCR

T91

GEMOS

SCR

T92

GEMOS

SCR

T93

GEMOS

SCR

T94

GEMOS

SCR

T95

GEMOS

SCR

T96

GEMOS

SCR

T97

GEMOS

SCR

T98

GEMOS

SCR

T99

GEMOS

SCR

T100

GEMOS

SCR

T101

GEMOS

SCR

T102

GEMOS

SCR

T103

GEMOS

SCR

T104

GEMOS

SCR

T105

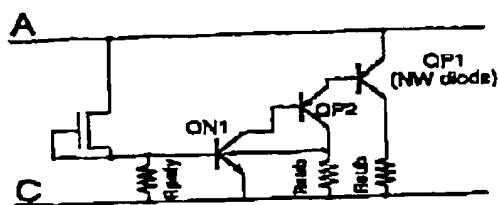
GEMOS

Exhibit B

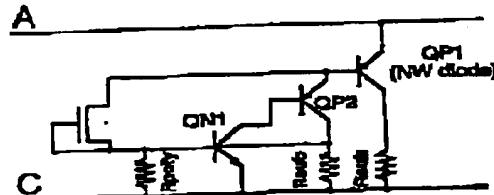
TSB CMOS2 RF ESD Test Chip

page 11 of 18

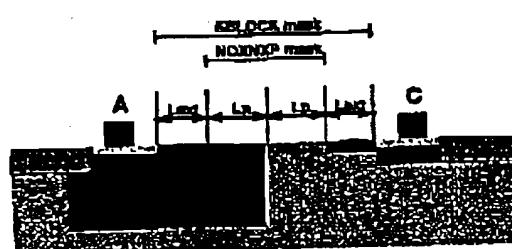
## GGSCR Structures



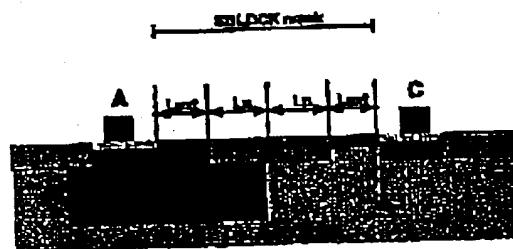
GGSCR with direct triggering (NMOS connected before diode-QP1) - Type A



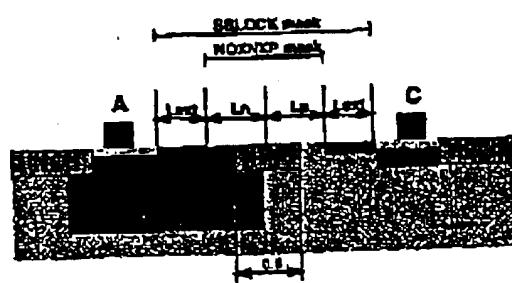
SCR with indirect triggering (NMOS connected after diode-QP1) - Type B



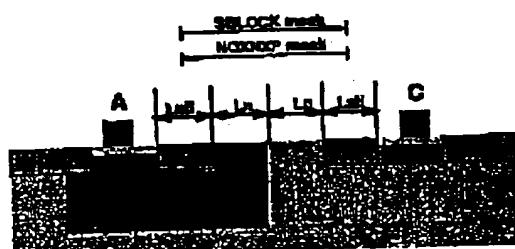
Standard GGSCR



GGSCR with STI and S/D extensions



GGSCR with center STI



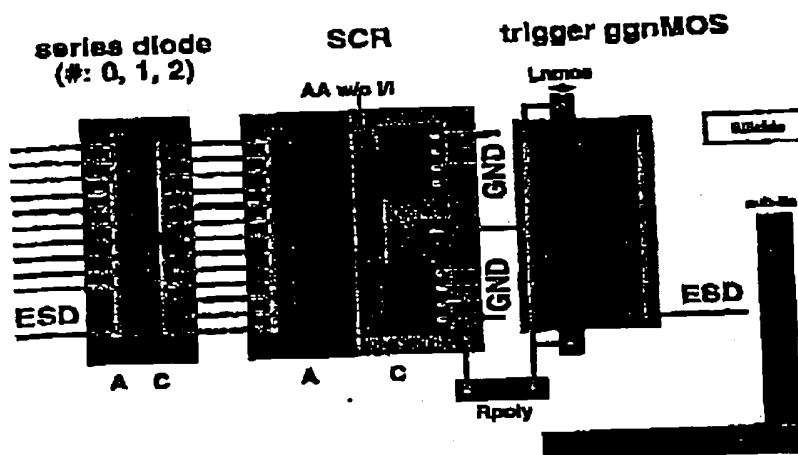
GGSCR with double STI to suppress the S/D extensions

Sarnoff Proprietary

EXHIBIT C

TSB CMOS2 RF ESD Test Chip

page 13 of 19



Layout example of GGSSCR - not drawn to scale.

**Diodes**

Nwell Diodes



Pwell Diodes



Pwell Diodes, single sided



Diode Type	Diode ID	W (μm)	L (μm)	Diode Area	Measurement	Measurement
Medium	Ppdi: A, C	2x20	0.00			
0.51	13.14				double-sided, PW	TLP, DC (bottom)
0.51	13.18	2x20	0.01		double-sided, PW	TLP, DC (bottom)
					single-sided, PW	TLP, DC (bottom)
		17.18	2x20	0.01	single-sided, PW	TLP, DC (bottom)
AS		4	0.00		double-sided, PW	TLP, DC (bottom)
AS		4	0.00		double-sided, PW	TLP, DC (bottom)
					single-sided, PW	TLP, DC (bottom)
51		44	0.00		single-sided, PW	TLP, DC (bottom)

**S-Parameter Calibration Structures**

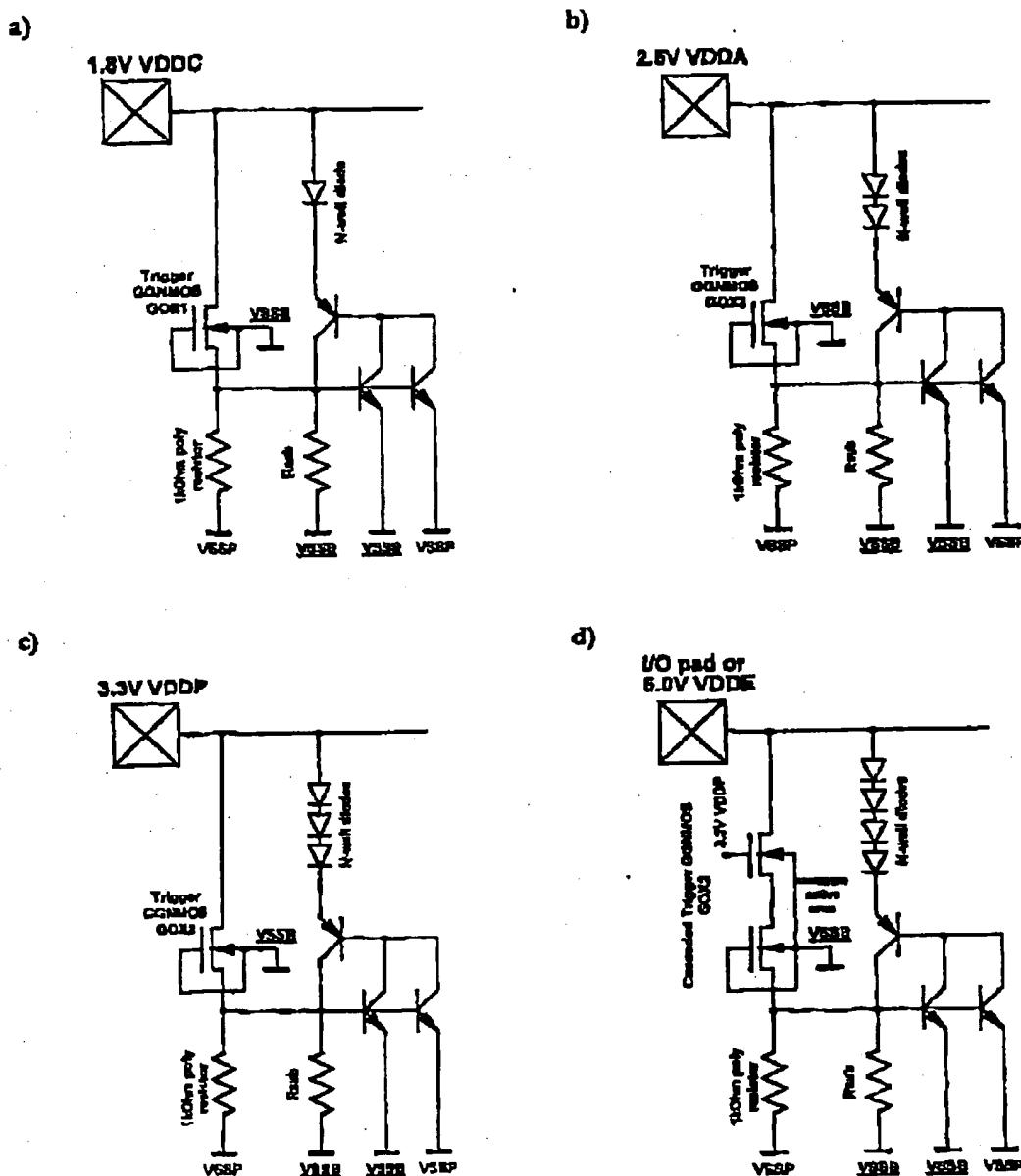
Calibration Structure Type	Calibration ID	W (μm)	L (μm)	Calibration Area	Measurement	Measurement
Medium	221	1000				
	513	1000				

Sarnoff Proprietary

EXHIBIT D

C10N 2kV ESD Design Guidelines, Bus Concepts, and Circuits

page 24 of 45



**Figure 11** Schematics of the GGSCR for the different supply voltage environments. Note the split NPN transistor of the SCR to accommodate ESD stress for both cases, versus VSSP (noisy source bus) and versus VSSB (quiet substrate bus).

EXHIBIT EDesign rules SCR:

- $W \geq 50\mu m$  (minimum requirement would be  $35\mu m$  but there needs to be a margin that includes voltage drops due to bus resistance such that the maximum voltage drop stays within the ESD design window)
- spacing from contact to silicide edge =  $0.6\mu m$
- spacing from silicide edge to diffusion edge =  $0.6\mu m$
- no-implant/no-STI-region: requires a special CAD layer operation - only the well implants are present
- spacing from diffusion edge to well-to-well junction (i.e. the no-implant/no-STI-region) =  $0.9\mu m$
- NPN-emitter and trigger taps intermittent (3 segments for a  $50\mu m$ -wide SCR with 2 trigger taps, no trigger taps at device extremities), local substrate connections not adjacent to trigger taps but shifted

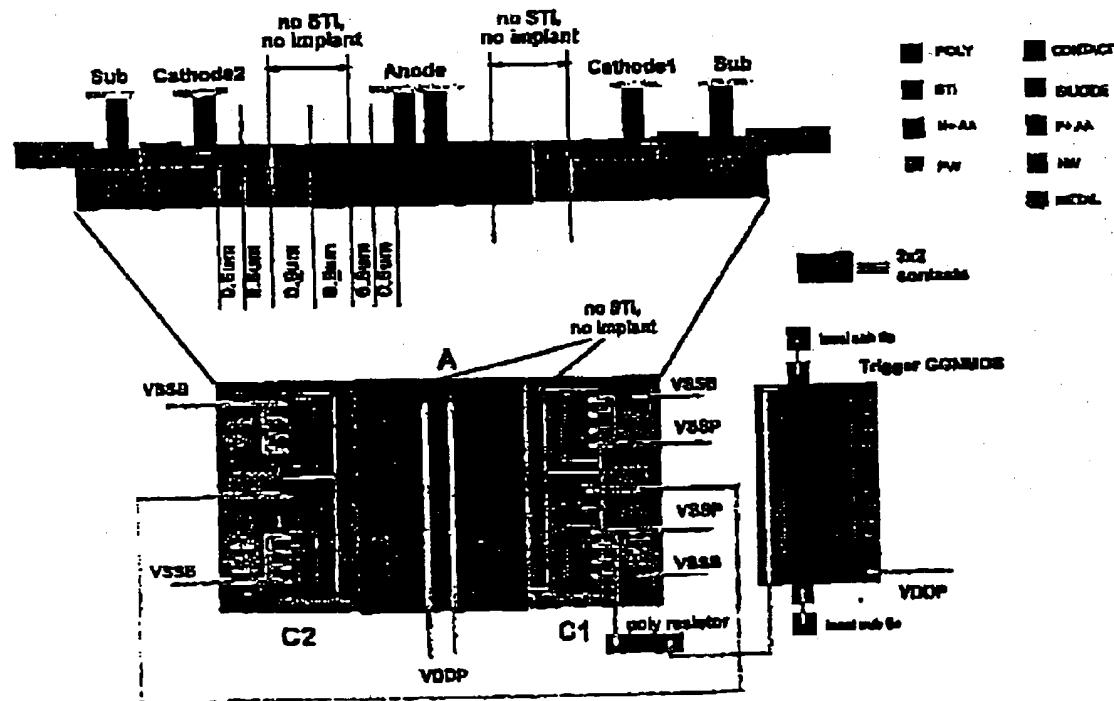


Figure 12 Cross-sectional view and layout details of the OGSCR.